What is claimed is:

1. A method for forming an epi-channel of a p-channel metal-oxide-semiconductor (pMOS) device, comprising the steps of:

forming a channel doping layer beneath a surface of a semiconductor substrate through a dual doping of dopants having different diffusion rates;

performing an annealing process for activating the dopants ion-implanted into the channel doping layer;

performing a surface treatment for removing a native oxide layer formed on a surface of the channel doping layer; and

growing a silicon epi-layer on the channel doping layer through a selective epitaxial growth.

2. The method as recited in claim 1, wherein the step of forming the channel doping layer includes further the steps of:

ion-implanting a first n-type dopant; and

ion-implanting a second n-type dopant having a diffusion rate higher than that of the first n-type dopant.

3. The method as recited in claim 2, wherein the first n-type dopant is As or Sb and the second n-type dopant is P.

4. The method as recited in claim 1, wherein the step of performing the annealing process is selected from either a rapid thermal annealing (RTA) or a spike RTA (SRTA).

5. The method as recited in claim 4, wherein the RTA is proceeded at a temperature ranging from about 600 °C to about 1050 °C, and the SRTA is performed at a temperature ranging from about 600 °C to about 1150 °C.

6. The method as recited in claim 1, wherein the surface treatment is performed at an atmosphere of hydrogen.

7. A method for fabricating a pMOS device, comprising the steps of:

forming an n-type channel doping layer beneath a surface of a semiconductor substrate through a dual doping of dopants having different diffusion rates;

performing a surface treatment for removing a native oxide layer formed on a surface of the n-type channel doping layer;

growing a silicon epi-layer on the n-type channel doping layer through a selective epitaxial growth;

forming sequentially a gate insulating layer and a gate electrode on a predetermined region of the silicon epi-layer through deposition and patterning processes;

forming a highly concentrated p-type source/drain extension region in a predetermined portion of the

semiconductor substrate beneath lateral sides of the gate electrode;

forming a spacer at lateral sides of the gate electrode; and

forming a highly concentrated p-type source/drain region electrically connected to the source/drain extension region.

8. The method as recited in claim 7, wherein the step of forming the n-type channel doping layer includes further the steps of:

ion-implanting a first n-type dopant; and

ion-implanting a second n-type dopant having a diffusion rate higher than that of the first n-type dopant.

9. The method as recited in claim 8, wherein the first n-type dopant is As or Sb, and the second n-type dopant is P.

10. The method as recited in claim 7, wherein the annealing process is selected any one from a rapid thermal process (RTA) and a spike RTA (SRTA).

11. The method as recited in claim 10, wherein the RTA is proceeded at a temperature ranging from about 600 °C to about 1050 °C, and the SRTA is performed at a temperature ranging from about 600 °C to about 1150 °C.

12. The method as recited in claim 7, wherein the surface treatment is carried out at an atmosphere of hydrogen.

13. The method as recited in claim 7, further comprising the step of forming an elevated source/drain region on the p-type source/drain region through a selective epitaxial growth.

14. A pMOS device, comprising:

a semiconductor substrate;

a channel doping layer being formed in a surface of the semiconductor substrate and being dually doped with dopants having different diffusion rates;

a silicon epi-layer being formed on the channel doping layer, whereby constructing an epi-channel along with the channel doping layer;

a gate insulating layer formed on the silicon epi-layer;

a gate electrode formed on the gate insulating layer;

a source/drain extension region highly concentrated and formed in the semiconductor substrate of both lateral sides of the epi-channel; and

a source/drain region electrically connected to the source/drain extension region and deeper than the source/drain region.

15. The pMOS device as recited in claim 14, the channel doping layer is dually doped with the first n-type dopant and the second n-type dopant having a higher diffusion rate than that of the first n-type dopant.

16. The pMOS device as recited in claim 15, wherein the first n-type dopant is As or Sb, and the second n-type dopant is P.

17. The pMOS device as recited in claim 14, wherein the channel doping layer is formed to have a thickness ranging from about 10 nm to about 50 nm.

18. The pMOS device as recited in claim 14, the silicon epi-layer is formed to have a thickness ranging from about 5 nm to about 30 nm.